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Cooperative Control of Multi-Master-Slave Islanded Microgrid with Power Quality Enhancement Based on Conservative Power Theory

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Abstract--Cooperative control of power converters in a microgrid offers power quality enhancement at sensitive load buses. Such cooperation is particularly important in the presence of reactive, nonlinear and unbalanced loads. In this paper, a multi-master-slave-based control of Distributed Generators (DGs) interface converters in a three-phase four-wire islanded microgrid using the Conservative Power Theory (CPT) is proposed. Inverters located in close proximity operate as a group in master-slave mode. Slaves inject the available energy and compensate selectively unwanted current components of local loads with the secondary effect of having enhanced voltage waveforms while masters share the remaining load power autonomously with distant groups using frequency droop. The close proximity makes it practical for control signals to be communicated between inverters in one group with the potential to provide rapid load sharing response for mitigation of undesirable current components. Since each primary source has its own constraints, a supervisory control is considered for each group to determine convenient sharing factors. The CPT decompositions provide decoupled current and power references in abc-frame, resulting in a selective control strategy able to share each current component with desired percentage among the microgrid inverters. Simulation results are presented to demonstrate the effectiveness of the proposed method.

Index Terms--Active Power Filter (APF), Conservative Power Theory, Cooperative Control, Distributed Generation, Four-leg Inverter, Microgrid, Power Quality Improvement.

I. INTRODUCTION

DISTRIBUTED Generation (DG) systems and microgrids are becoming more and more important as the penetration level of renewable energy increases in power grid [1]-[3]. Intelligent converters interfacing the generation sources and grid are an essential part of such DG and microgrid systems. These interfacing converters can be classified into current-controlled inverters to inject desired current into the grid and voltage-controlled inverters to establish and regulate voltage under autonomous or islanded operating conditions [4].

Various schemes have been proposed in the literature for

parallel connection of converters which can be roughly divided into two categories: communication-based [5]-[12] and non-communication-based schemes [5], [6], [13]. Communication-based control of a microgrid system relies on sharing control information among different inverters. When inverters are located in close proximity of each other, methods such as central mode control, master-slave mode control and distributed control can be applied [5]-[7]. In the central mode, the control method requires common synchronization signals and current sharing modules [5]. The PLL circuit of each module can ensure the consistency between the frequency and phase of the output voltage and the synchronization signal. Also, the current sharing modules observe the total load and each module tracks the average current to achieve equal current distribution. This method directly adds current error to each inverter unit as a compensation component of the voltage reference in order to eliminate the differences among their output currents. However, this control scheme must include a centralized controller, which makes difficult to expand the system. In the distributed control method, also represented as the instantaneous average current sharing method, no central controller is needed [5], [8]. All of the inverters take part in the voltage, frequency, as well as the current regulation, while the average current is the shared information for each module. Average current sharing requires a current sharing bus and reference synchronization for the voltage. An additional current control loop is used to enforce each converter to track the same average reference current, provided by the current sharing bus. Gain scheduler is introduced in instantaneous average current sharing scheme, to improve the current and power sharing for a condition, where the line impedance is different among the inverters [9]. In the master/slave control method, the master inverter operates as a voltage source to regulate the system voltage, while the slave inverter acts as a current source to track the output current of the master in order to achieve equal current distribution [5], [10]-[12]. Based on this scheme, inverters do not need any PLL for synchronization since these units are communicated with the master units.

The close proximity makes it practical for control signals to be communicated between inverters with the potential to provide better controllability in terms of fast response to load changes, better voltage regulation, and proper power sharing [5], [14]. However, communication-based approaches have

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some drawbacks including: the need for high-bandwidth communication channels, especially in case of harmonics compensation which can be impractical and costly in microgrids with long connection distances between inverters; and the presence of a unit acting as a central control or a master which creates a single point of failure.

Non-communication-based control relies on the ability of individual DG units to regulate the output voltage and frequency while sharing the active and reactive power demands. A simple non-communication-based power sharing strategy can be realized in the sense of frequency and voltage droop method [13]. The advantage of the droop method is that it does not require communication signals amongst units in parallel; thereby enhancing the reliability of the system at the price of permitting a small error. Some low bandwidth communication can be added to the system so that voltage amplitude and frequency can be adjusted and generators scheduling is allowed. In [15] droop control has applied to control not only active and reactive power but also unbalance and harmonic power. A droop control method based on negative sequence reactive power has been presented in [16] for voltage unbalance compensation. In [17] a capacitive virtual impedance scheme has been presented for LCL-terminated voltage source inverters. The aim of this scheme is to compensate output voltage distortion. However, enhancement of filter output voltage quality is achieved at the price of voltage distortion increase at filter capacitance. Furthermore, for a proper load sharing, resistive virtual impedances are added which distorts again output voltage as a result of voltage drop on the virtual resistances. In [18], the secondary control level is applied to manage the selective compensation of sensitive load bus voltage unbalance and harmonics by sending proper control signals to the primary level. First, virtual resistances for fundamental negative sequence and harmonic components are added to improve the current sharing. The improvement is achieved at the expense of voltage distortion increase at DG units terminals and consequently at sensitive load. Furthermore, the addition of these virtual resistances leads to coupling between fundamental positive sequence and other components. After activating selective compensation, sensitive load bus voltage quality is improved. However, the compensation is achieved by the increase of output voltage distortion of DGs. Thus, considering the required power quality, possible practical limitations are still remained.

Communication should be used to the extent that is practicable in a given environment [14]. Therefore, inverters located in close proximity could have access to high-bandwidth communication links to provide rapid load sharing response for ancillary functions including voltage support, harmonic mitigation, and unbalance compensation. However, the impracticality of communication between inverters at remote nodes is recognized and the sharing between these groups is accomplished through the conventional voltage and frequency droop methods. Therefore, in this paper a multi-master-slave-based control of DGs in an islanded microgrid is proposed in which DGs connected to a common bus or located in close

proximity operate as a group in master-slave mode, with slaves injecting their available energy and mitigate unwanted or non-active current components of their local nonlinear or unbalanced loads and masters sharing autonomously the remaining load power with distant groups using droop control. This way, the non-active load current components in each group are compensated locally by the slaves with access to high-bandwidth communication links. As the secondary effect, the enhancement of voltage quality at master inverters terminal and load buses is achieved simultaneously. However, in contrast to conventional master-slave control strategy, where slave units track the current reference provided by the master in order to achieve equal current distribution [5], the slave reference currents in this strategy are synthesized from the load currents based on the CPT. The slave units in each group can track the load current at the voltage fundamental frequency which is controlled by the master unit without requiring PLL circuits for the synchronized operation. Since supplying the non-active load current components result in severe voltage distortion at the slave DG units (SDG) terminals or overloading the units interface converters, cooperation of slave units operating only as APF (SAPF) is also required [19]. Supervisory control checks the SDG output voltage THD and if they exceed their maximum allowable value, commands the SAPF to cooperate for reduction of the SDG compensation duty and consequently voltage distortion at their terminals. The major contributions of this paper can be summarized as follows:

- 1) In contrast to conventional master-slave control strategy, the slave reference currents in this strategy are synthesized from the load currents based on the CPT.
- 2) The non-active load current components in each group are compensated locally by the slaves with access to high-bandwidth communication links.
- 3) Conventional droop control with resistive line impedance compensation is implemented to have decoupled active and reactive power controllers and proper active power sharing among DGs.
- 4) Enhancement of the voltage quality at master inverters terminals and also the load buses is achieved simultaneously as the secondary effect of the non-active load current compensation.
- 5) The slave units do not require PLL circuits for the synchronized operation providing a means for easy expansion of this type of parallel-connected inverters.
- 6) The cooperation between the SDG and the SAPF is discussed.

Rest of this paper is organized as follows. Section II presents the modeling of the current-controlled and voltage-controlled DG inverters in the stationary reference frame. In Section III, a brief review of the CPT for three-phase circuits is presented following by the load current sharing strategy among DG interface converters. Section IV is dedicated to the simulation results of the proposed cooperative control strategy and the conclusion of this paper is presented in Section V.

II. MODELING OF THE SLAVE AND MASTER DG INVERTERS

Fig. 1 shows the single line diagram of the proposed multi-

master-slave-based islanded microgrid, including groups, A, B, C, D, etc. Group A control structure is shown for illustration. It is composed of a master and a number of slave electronically interfaced DGs. The master Voltage Source Inverter (VSI) is controlled as a voltage-controlled inverter to establish the load voltage and, simultaneously, to share load current components with the current-controlled or slave VSI-based DGs. Regarding load sharing, it should be noted that the conventional droop method for active and reactive power control is developed based on the predominantly inductive line impedance. However, in low voltage microgrid applications this assumption is challenged since low voltage distribution lines have complex values of the line impedance leading to coupling between P and Q [5], [20]. This, in turn, leads to poor performance of the system if conventional droop control method is applied. To deal with this problem, various methods such as voltage active power droop and frequency reactive power boost (VPD/FQB) droop, complex line impedance based droop, resistive-inductive virtual impedance, and virtual frame transformation have been introduced [5]. In this paper, compensation of resistive line impedance is implemented to decouple P and Q by a feedback loop which adds the resistive voltage drop across the line impedance to the reference voltage. The gain of this feedback loop is equal to the resistive impedance of the line causing to have decoupled active and reactive power controllers and proper active power sharing among DGs.

Fig. 1 shows the implementation of this current feedback loop. For the sake of simplicity, all VSIs are assumed to have the same topology. Each unit consists of a four-leg VSI, three legs connected through a three-phase LC-filter and equal line

impedances to the local network loads, and neutral wire is connected to the fourth leg. The inductance and capacitance of the output filter are L_f and C_f , respectively, and R_f models the ohmic loss of the inductor. The effect of DG unit is represented by a DC voltage source, connected in parallel with the VSI DC-link capacitor. The parameters of the microgrid system are illustrated in Table I.

TABLE I
Microgrid Parameters.

Parameters	Values
Nominal phase RMS voltage	127 V
Grid frequency, f	60 Hz
Maximum power output of inverters	10 kVA
Switching frequency, f_s	20 kHz
Output filter inductor, L_f	3 mH
Output filter resistor, R_f	0.1 Ω
Output filter capacitor of Masters, C_{fm}	30 μ F
Output filter capacitor of Slaves, C_{fs}	2.5 μ F
DC-link voltage, V_{dc}	700 V
Carrier amplitude voltage	5 V
Sampling Period, T_s	(1/20000) s

An accurate and robust current control scheme is devised with a fast dynamic response, showing that i_a , i_b , i_c and i_n can rapidly track their respective reference commands i_{ta}^* , i_{tb}^* , i_{tc}^* and i_{tn}^* . It should be pointed out that i_{tn}^* is determined as $i_{tn}^* = -(i_{ta}^* + i_{tb}^* + i_{tc}^*)$. The block diagram of the control strategy is illustrated in Fig. 2. Fig. 2(a) depicts the closed-loop current control structure which regulates the output current of the slaves, where $G_{oi}(s)$, $C_i(s)$ and $G_{ci}(s)$ are the open-loop, the controller and the closed-loop transfer functions of the current control scheme, respectively.

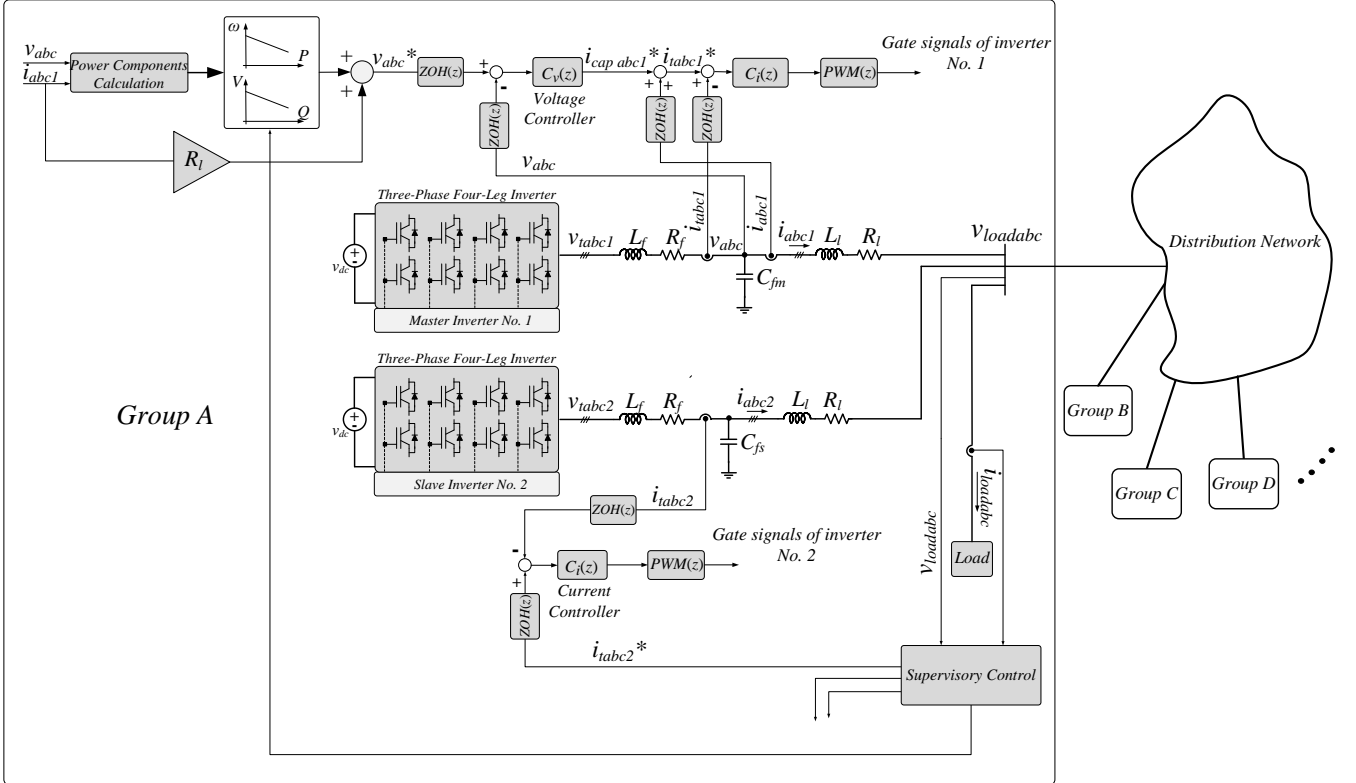


Fig. 1. Proposed multi-master-slave-based autonomous microgrid, including groups, A, B, C, D, etc.

The transfer function $G_{oi}(s)$ of the open-loop current controller scheme is obtained as in (1). The current controller, $C_i(s)$, is chosen to be a Proportional Integral (PI) compensator as in (2) where the parameters of k_p and k_i are the proportional and integral gains of the compensator, respectively. The crossover frequency of the current controller is chosen to be $f_{ci} = 2$ kHz and the phase margin ϕ_{PMi} is selected to be 60° . We can compute that $k_p = 0.465$ and $k_i = 3399$. To digitally implement the control system in the z-domain, the PI controller of (2) is discretized by the backward Euler method with a sampling time of T_s that is also the switching period. Therefore, the controller transfer function $C_i(z)$ can be expressed as (3). For $T_s = 1/(20 \text{ kHz})$, the parameters in the z-domain controller transfer function of (3) are calculated as $n_1 = 0.635$, $n_0 = -0.465$, $d_1 = 1$ and $d_0 = -1$. The closed loop transfer function of the current control scheme $G_{ci}(s)$ is shown in (4).

Master inverters in each group are controlled in voltage control mode to establish their local load bus voltage while, at the same time, share the load current components with the slave inverters. Fig. 2(b) illustrates the control scheme for regulating v_{abc} . A feed-forward based control strategy is developed in a multiloop voltage control scheme with the current-controlled scheme of Fig. 2(a) as the inner loop to regulate load voltage/frequency in a wide range of load conditions [21]. Applying the filter inductor current as the inner loop feedback variable, the inductor current is then measured directly, allowing overcurrent protection to be easily added to the control. In Fig. 2(b), $v_{abc}(s)$ is controlled by $i_{cap}^*(s)$ which is the output of the voltage controller. Then, the transfer function of the plant is obtained as in (5). $G_{ov}(s)$ in (6) is the open-loop transfer function of the voltage control scheme, where $C_v(s)$ is the controller of the outer voltage control loop. A PI compensator as in (2) is chosen for tracking the reference voltage in this plant.

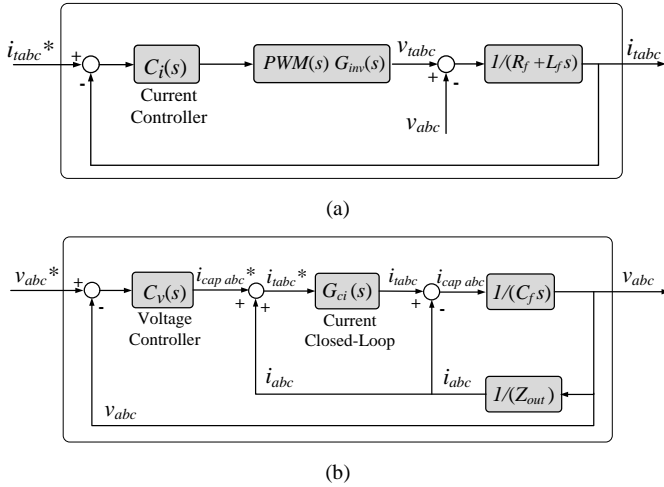


Fig. 2. (a) Block diagram of the current control scheme; (b) Block diagram of the voltage control scheme.

$$G_{oi}(s) = \frac{PWM(s)G_{inv}(s)}{R_f + sL_f} C_i(s). \quad (1)$$

$$C_i(s) = \frac{k_p s + k_i}{s}. \quad (2)$$

$$C_i(z) = \frac{n_1 z^1 + n_0}{d_1 z^1 + d_0}. \quad (3)$$

where

$$n_1 = k_i T_s + k_p, n_0 = -k_p, d_1 = 1 \text{ and } d_0 = -1.$$

$$G_{ci}(s) = \frac{i(s)}{i^*(s)} = \frac{C_i(s) PWM(s) G_{inv}(s)}{L_f s + R_f + C_i(s) PWM(s) G_{inv}(s)}. \quad (4)$$

$$G_{Plant}(s) = \frac{v(s)}{i_{cap}^*(s)} \approx G_{ci}(s) \frac{1}{C_f s}. \quad (5)$$

$$G_{ov}(s) = G_{Plant}(s) C_v(s). \quad (6)$$

$$v(s) = \frac{C_v(s) C_i(s) PWM(s) G_{inv}(s)}{L_f C_f s^2 + C_f R_f s + C_f C_i(s) PWM(s) G_{inv}(s) s + C_v(s) C_i(s) PWM(s) G_{inv}(s) + 1} v^*(s) - \frac{R_f + L_f s}{L_f C_f s^2 + C_f R_f s + C_f C_i(s) PWM(s) G_{inv}(s) s + C_v(s) C_i(s) PWM(s) G_{inv}(s) + 1} i_{abc}.$$

For $f_{cv} = 0.7 \text{ kHz}$ and phase margin of 50° , we can calculate that $k_p = 0.092$ and $k_i = 258$. The voltage PI controller $C_v(s)$ is also discretized by the backward Euler method for digital implementation. For $T_s = 1/(20 \text{ kHz})$, the parameters in the z-domain controller transfer function of $C_v(z)$ are calculated as $n_1 = 0.105$, $n_0 = -0.092$, $d_1 = 1$ and $d_0 = -1$. Equation (7) depicts the output voltage dependence on both the reference voltage and the inverter output current.

III. LOAD CURRENT SHARING STRATEGY AMONG DG INVERTER UNITS

To develop selective current injection in an isolated microgrid with unbalanced and distorted voltage operating conditions, the CPT decomposition technique is used, enabling control of each current component with desired sharing percentage among the microgrid inverters. The CPT first proposed by Tenti et al. [22], is a time-domain-based decomposition technique valid for single- and poly-phase systems, with or without neutral current, independent from voltage operating conditions (sinusoidal or non-sinusoidal) [23], [24]. CPT offers an orthogonal decomposition of current and power in the neutral (abc) frame, with respect to terms directly related to electrical characteristics, such as: average active power transfer, reactive energy, unbalanced loads and nonlinearities. Thus, let us consider a generic poly-phase circuit under periodic operation. In the following, instantaneous and RMS quantities are indicated with lowercase and uppercase symbols, respectively, vector quantities (i.e., collective values) with boldface symbols and each phase of the system is denoted by the subscript 'm'.

- balanced active currents (i_{am}^b), have been determined as the minimum currents needed to convey total active power ($P = \sum_{m=1}^M P_m$) absorbed at the PCC;
- balanced reactive currents (i_{rm}^b), have been defined as the minimum currents needed to convey total reactive energy ($W = \sum_{m=1}^M W_m$) absorbed at the PCC;
- void currents (i_{vm}), which are related to the nonlinear behavior between voltages and load currents;
- unbalanced currents ($i_m^u = i_{am}^u + i_{rm}^u$), which are related to the unbalanced load behavior;

- non-active currents (i_{nam}), which represent all the unwanted terms of the load currents ($i_{nam} = i_{rm}^b + i_{vm} + i_m^u$).

By definition, the collective RMS current can be split into:

$$I^2 = (I_a^b)^2 + (I_{na})^2 = (I_a^b)^2 + (I_r^b)^2 + (I^u)^2 + (I_v)^2, \quad (8)$$

Thus, the apparent power may be calculated as:

$$A^2 = V^2 \cdot I^2 = P^2 + Q^2 + N^2 + D^2, \quad (9)$$

where $P = V \cdot I_a^b$ is the active power, $Q = V \cdot I_r^b$ is the reactive power, $N = V \cdot I^u$ is the unbalance power and $D = V \cdot I_v$ is the distortion power.

Unbalanced or nonlinear loads result in the deterioration of voltage waveforms at load buses which is the direct consequence of voltage drop across the line impedances. In this paper, the objective of the multi-master-slave-based cooperative control is the network at the load buses is seen resistive from the point of view of the master units that regulates the load buses voltages. This way, master units will be able to establish good quality voltages at load buses. To achieve this, master inverters need to provide only the balanced active current components of the loads to prevent the local load bus voltage in each group from distortion. This way, the non-active load current components in each group compensate locally by the slaves located in close proximity with access to high-bandwidth communication links. The slave units are current-controlled and the output current of slave units tracks the current reference distributed by the supervisory control. The supervisory control in each group has access to the load current, and act as operator/management unit. It decomposes the load current components into different orthogonal current terms, directly related to electrical characteristics, based on the CPT and assigns each slave to supply different current components and, therefore, the master inverter supplies the remaining load current simultaneously. Since the slave reference currents are synthesized from the load currents, the slave units in each group can track the load current at the voltage output frequency which is controlled by the master unit. Consequently, the slave units do not require PLL circuits for the synchronized operation providing a means for easy expansion of this type of parallel-connected inverters.

In this study, the design strategy is to assign the non-active load current compensation duty to the SDG to lessen capital investment. However, since the generation and consumption conditions in a microgrid can change considerably, it is probable that the compensation by the SDG leads to overloading of them or excessive voltage distortion at their terminals. In these conditions, SAPF can be considered to be installed at the load buses to address these requirements. A general structure of microgrid with DGs and units operating only as APF are presented in [19]. The cooperation in this paper is built on the following rules:

- 1) The SDG have priority in non-active load current compensation to utilize the available capacities of their interfacing converters while the voltage distortion rate of their terminals and the used capacity of their converters are within the rated limit.

- 2) While the SDG are compensating loads non-active currents, their output voltage distortions should not exceed from their maximum allowable values. To apply this constraint, voltages THDs of the SDG terminals are evaluated.
- 3) The SDG interfacing converters should not be overloaded while compensating loads non-active currents. To apply this constraint, output currents of DG units are evaluated.
- 4) Compensation task of the SAPF should be shared between them so that none of them are overloaded. Like DG units rating power constraints, their output current are evaluated for this purpose.

Voltage THD at the DG terminals and used capacity of the interface converters are computed for each unit and if cooperation is required, proper signal is calculated in the supervisory control and sent to the SAPF to start cooperating for reduction of the DGs compensation duty and consequently voltage distortion at their terminals. Note that the SAPF only cooperate with those DGs needing cooperation. If a group does not compensate entirely its non-active currents, then those currents will be shared by master units. Note that the slave units in each group are aimed to mitigate just their local load non-active currents. The slave units are not supposed to mitigate other unwanted currents that their information is not revealed for their group supervisory control. As mentioned before, conventional droop control with resistive line impedance compensation is applied to share the load active power components between master inverters. This is due to impracticality of communication between groups located at remote nodes. The applied droop control shows excellent performance for active power sharing between master units irrespective of the non-active currents mitigation by the slaves units.

IV. SIMULATION RESULTS

To evaluate the dynamic performance of the proposed cooperative control strategy, the schematic diagram of the multi-master-slave-based autonomous microgrid of Fig. 3, was simulated in PSIM software. The CPT current decomposition has been implemented by means of an algorithm programmed in a standard C compiler, while the controllers were implemented using z-domain transfer functions. Here, the system under study consists of two groups of inverters, groups A and B. Each group involves three sets of four-leg VSI-based DG units connected through line impedances to their local network loads. L_l and R_l represent the inductance and resistance of the inter-group line impedance that connects groups A and B inverters together, respectively. L_{lA} , L_{lB} , R_{lA} , and R_{lB} represent the inductance and resistance of the group A and B line impedances, respectively.

A. Compensation of non-active load current

The load circuit used in group A and group B is shown in Fig. 4; it contains balanced and unbalanced linear and non-linear loads. Originally, the system is under load configuration of Fig. 4 for each group. At $t=0.9s$, another set of load circuit of Fig. 4 is switched on in group A resulting in load current increment by twice in this group (see Figs. 8(a) and 8(b)). Load and line impedance parameters are provided in Table II.

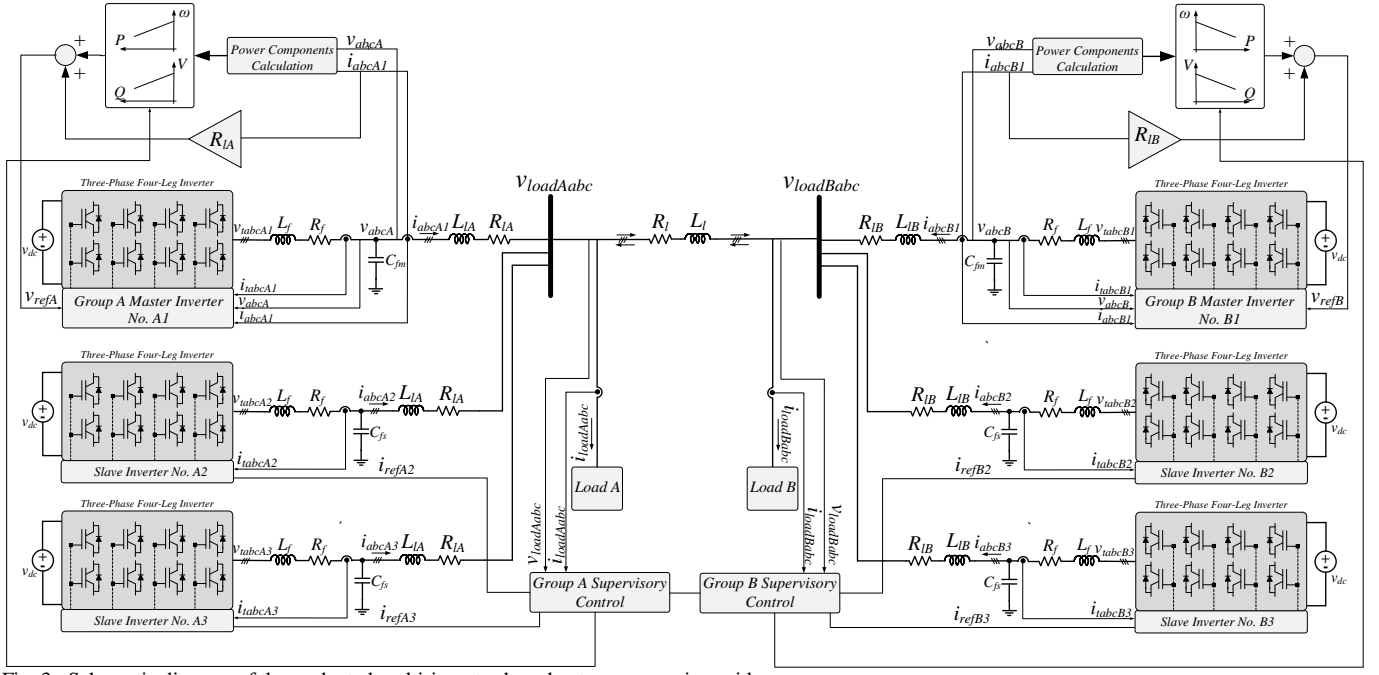


Fig. 3. Schematic diagram of the evaluated multi-inverter-based autonomous microgrid.

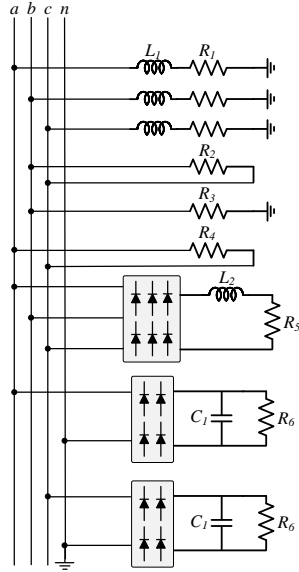


Fig. 4. Schematic diagram of the configurable load.

TABLE II
Load and Line Impedance Parameters.

Parameters	Values
Load inductor, L_1	50 mH
Load inductor, L_2	4 mH
Load capacitor, C_1	220 μ F
Load resistor, R_1	20 Ω
Load resistor, R_2	80 Ω
Load resistor, R_3	100 Ω
Load resistor, R_4	70 Ω
Load resistor, R_5	40 Ω
Load resistor, R_6	50 Ω
Groups A and B Line inductor, L_{1A} and L_{1B}	1 mH
Groups A and B Line resistor, R_{1A} and R_{1B}	5 Ω
Inter groups line inductor, L_l	1 mH
Inter groups line resistor, R_l	0.1 Ω

Fig. 5 presents groups A and B master inverter voltage waveforms while Fig. 6 and Fig. 7 present the group A and B load buses voltages and currents and the current waveforms in each inverter before and after load bus voltage enhancement ($t=0.3s$), respectively. In groups A and B:

- \underline{v}_{refA} and \underline{v}_{refB} : reference voltages,
- v_{abcA} and v_{abcB} : capacitor voltages,
- i_{abcnA1} and i_{abcnB1} : output currents of master inverters A1 and B1,
- \underline{i}_{refA2} and \underline{i}_{refB2} : reference currents of slave inverters A2 and B2,
- i_{abcnA2} and i_{abcnB2} : output currents of slave inverters A2 and B2,
- \underline{i}_{refA3} and \underline{i}_{refB3} : reference currents of slave inverters A3 and B3,
- i_{abcnA3} and i_{abcnB3} : output currents of slave inverters A3 and B3,
- $v_{loadAabc}$ and $v_{loadBabc}$: voltages of loadA and loadB,
- $i_{loadAabc}$ and $i_{loadBabc}$: currents of loadA and loadB.

From Fig. 5 to Fig. 7, until $t=0.3s$, the slave inverters gating signals are blocked, and controllers are inactive. Therefore, the local loads are supplied by the group A and B master inverters specified by i_{abcnA1} and i_{abcnB1} with the droop ratio of ($k_{pA1} = \frac{1}{2} k_{pB1}$) and ($k_{qA1} = k_{qB1}$) provided by the respective supervisory control (see Figs. 8(a)-8(f)). Since the loads are unbalanced and distorted, due to voltage drop across line impedances, the load buses voltages are also unbalanced and distorted which shows the necessity of voltage quality enhancement at load buses. Note that the master inverters supplies the neutral currents associated with single-phase loads through their fourth-legs, that is ($i_{nA1} = i_{loadAn}$) and ($i_{nB1} = i_{loadBn}$). The neutral currents include both linear and nonlinear loads among phases and neutral.

At $t=0.3s$, the gating signals of slave inverters are unblocked, controllers are enabled, and the inverters start to inject available energy. Group A slave inverters take one-third of the balance active current/power component of their own local load ($loadA$), each slave one-sixth, and Group B slave inverters take two-third of the balance active current/power component of their own local load ($loadB$), each slave one-third. To improve the load voltage quality, the provision of non-active components are also carried out by the slave inverters meaning that the master inverters need to supply the remaining balanced active component with the droop ratio of ($k_{pA1} = \frac{1}{2}k_{pB1}$). Consequently, since the slave inverters supply non-active current components, the master units see the network at the load buses, as a resistive network ensuring a good quality load bus voltage with THD reduction from 12% to 2%.

For this study, the void and unbalanced currents in groups A and B are supplied by slave inverters 2 and 3, respectively. The reference current provided by the group A supervisory control for these inverters are ($i_{refA2} = \frac{1}{6}i_a^b + \frac{1}{2}i_r^b + i_v$) and ($i_{refA3} = \frac{1}{6}i_a^b + \frac{1}{2}i_r^b + i_v$) of $loadA$. The reference current provided by the group B supervisory control for respective slave inverters 2 and 3 are ($i_{refB2} = \frac{1}{3}i_a^b + \frac{1}{2}i_r^b + i_v$) and ($i_{refB3} = \frac{1}{3}i_a^b + \frac{1}{2}i_r^b + i_v$) of $loadB$. It is observed from Fig. 6 and Fig. 7 that the master inverters no longer supplies the neutral currents associated with single-phase loads and the slave inverters take this task through their fourth-legs, that is ($i_{nA1} = 0$, $i_{nA2} + i_{nA3} = i_{loadAn}$) and ($i_{nB1} = 0$, $i_{nB2} + i_{nB3} = i_{loadBn}$). It is noted that in each group the slave inverter 2 supplies the non-linear part of neutral current associated with single-phase loads and the slave inverter 3 supplies the linear part of neutral current associated with single-phase loads.

Note that in [17], the capacitive virtual impedance scheme enhances the LCL-filter output voltage quality at the expense

of voltage distortion increase at filter capacitance, thus, in the cases that capacitor voltage quality is also important, a tradeoff should be made between capacitor and output voltage quality. In contrast to [17], [25], in this paper enhancement of master inverters terminals voltage quality and load buses voltage quality is achieved simultaneously as it is shown in Fig. 5 to Fig. 7 and no tradeoff is needed to be made between master inverters terminals and load buses voltages quality. It means the line impedances of master inverters will not distort their terminal voltages. For the SDG taking part in compensating loads non-active currents, if the output voltage THD exceeds the maximum allowable value due to compensation, proper signals are calculated in the supervisory control and sent to the SAPF to start cooperating for reduction of the SDG compensation duty and consequently voltage distortion at their terminals.

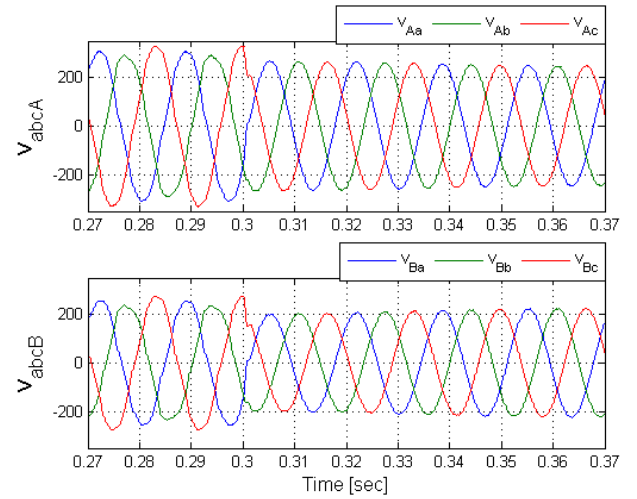


Fig. 5. Group A and B master inverters voltage waveforms before and after load bus voltage enhancement ($t=0.3s$).

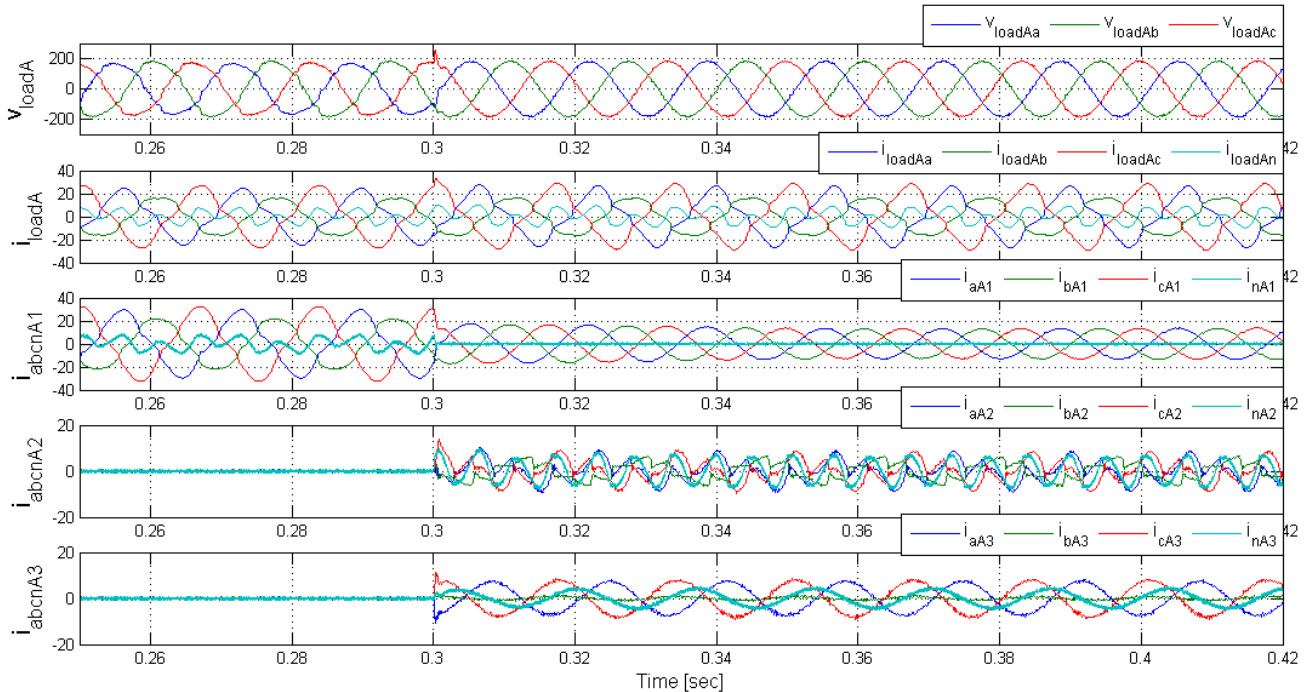


Fig. 6. Group A load bus voltage and current and the current waveforms in each inverter before and after load bus voltage enhancement ($t=0.3s$).

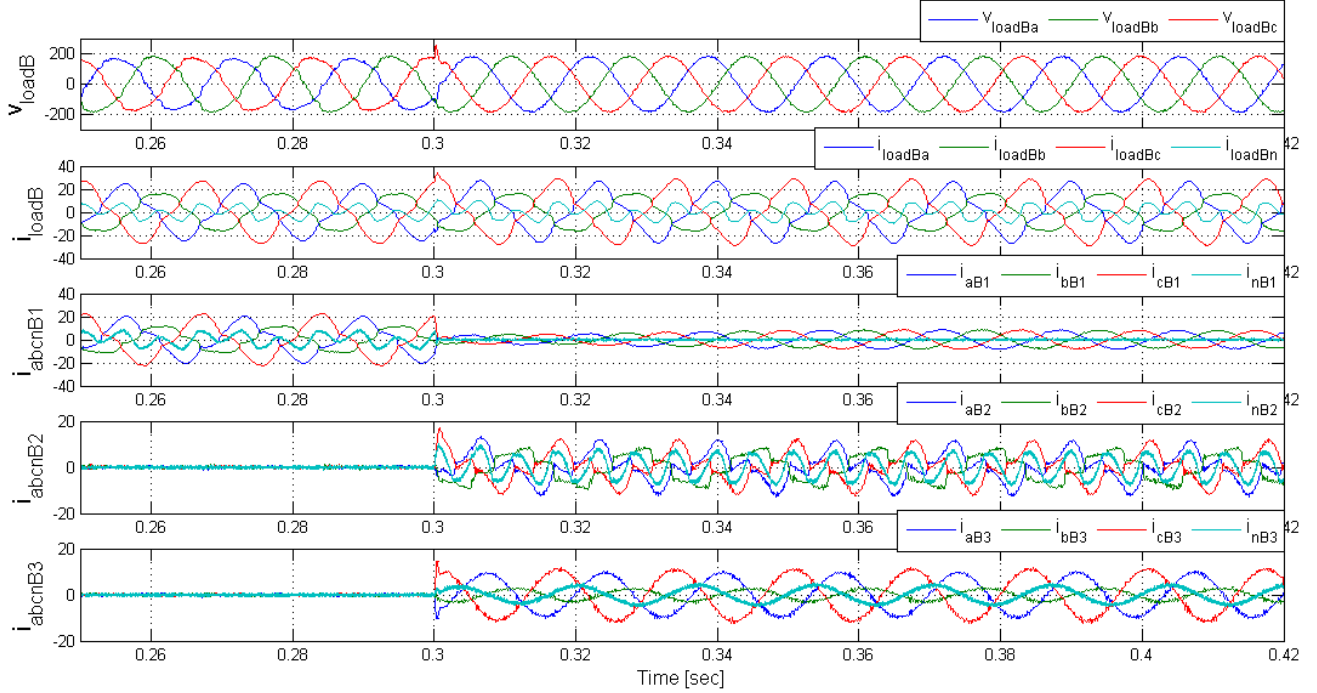


Fig. 7. Group B load bus voltage and current and the current waveforms in each inverter before and after load bus voltage enhancement ($t=0.3s$).

B. Sharing of load components among DG units

Fig. 8 illustrates the dynamic performance of the evaluated multi-inverter-based autonomous microgrid. Fig. 8(a) and Fig. 8(b) illustrates active, reactive, unbalance and distortion power components of the loads in groups A and B inverters, while Fig. 8(c) to Fig. 8(f) show those generated power components by inverters in each group, respectively. Originally, the system is under identical load configuration for each group. At $t=0.9s$, another set of load configuration is switched on in group A resulting in load current increment by twice in this group.

Fig. 8(c) shows the sharing of loads active power components (P_{loadA}) and (P_{loadB}) between groups A and B inverters. From Fig. 8(c), as it was mentioned before, until $t=0.3s$, all the load currents are supplied by the master inverters in each group. As the ratio of active droop line setting for master inverters is ($k_{pA1} = \frac{1}{2} k_{pB1}$), group A master inverter supplies twice the balanced active power of group B master inverter, ($P_{A1} = 2P_{B1}$). Therefore, group A master inverter not only supplies *loadA*, but also partially supplies *loadB* as it is shown by (P_{lineAB}) in Fig. 8(c).

At $t=0.3s$, slave inverters start injecting energy. Group A slave inverters takes one-third of the balance active power component of *loadA*, each slave one-sixth, and group B slave inverters takes two-third of *loadB*, each slave one-third. This way, group A master inverter, (P_{A1}), supplies two-third of *loadA* compared to group B master inverter, (P_{B1}), which supplies one-third of *loadB*. As a result, (P_{lineAB}) is zero meaning there is no active power transfer between groups A and B.

At $t=0.6s$ the supervisory control sets new ratio for master inverters active power droop slope as ($k_{pA1} = 2 k_{pB1}$) meaning that group B master inverter supplies twice the balanced active

power component as group A master inverter ($P_{B1} = 2P_{A1}$). Therefore, it not only supplies *loadB*, but also provides part of *loadA* in group A. Consequently, (P_{lineAB}) has negative value meaning the direction of active power transfer is from Group B to A.

At $t=0.9s$, another set of load configuration is switched on in group A resulting in load increment by twice in this group. It can be seen that group B master inverter still supplies twice the balanced active power of group A master inverter ($P_{B1} = 2P_{A1}$) as ($k_{pA1} = 2 k_{pB1}$). Note that groups A and B slave inverters now supplies equal amount of active power, as group B slave inverters is set to supply two-third of *loadB* considering *loadA* is now twice *loadB*. Since group A load consumes twice group B load, (P_{lineAB}) has negative value meaning the direction of active power transfer is from Group B to A.

At $t=1.2s$ the supervisory control sets new ratio for master inverters active power droop slope as ($k_{pA1} = k_{pB1}$) meaning that groups A and B master inverters share the same amount of active power components ($P_{A1} = P_{B1}$). (P_{lineAB}) is negative showing the power transfer is still from B to A, since group A load consumes twice group B load.

Fig. 8(d) shows the sharing of load reactive power component (Q_{loadA}) and (Q_{loadB}) among group A and B inverters. Originally, the system is under identical load configuration for each group. As the ratio of reactive droop line setting for master inverters is ($k_{qA1} = k_{qB1}$), group A and B master inverters share the total balanced reactive power component of *loadA* and *loadB* equally, i.e., ($Q_{A1} = Q_{B1}$), with each master inverter supplying its respective local load. As *loadA* and *loadB* are identical, (Q_{lineAB}) is negligible meaning that, except for reactive power losses over the inter groups line impedance, there is no reactive power transfer between groups A and B.

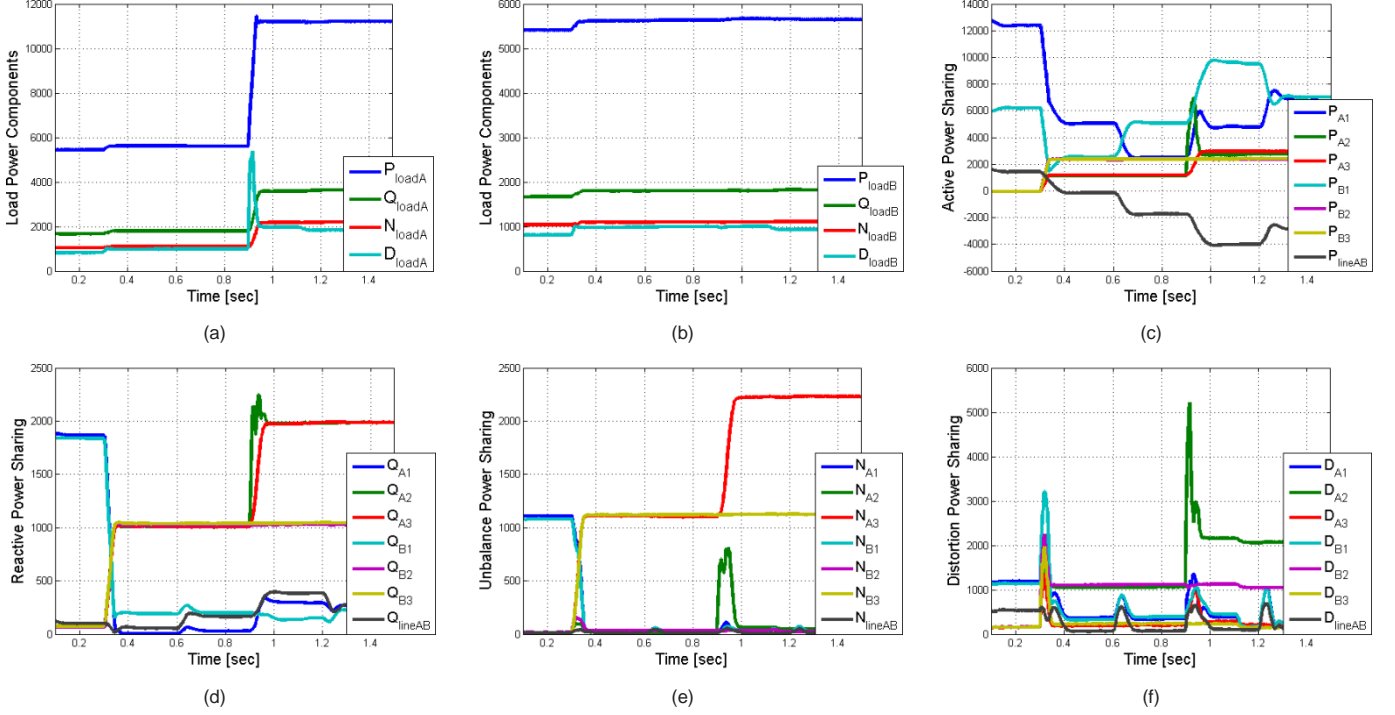


Fig. 8. (a) Group A Load power components; (b) Group B Load power components; (c) Active power sharing; (d) Reactive power sharing; (e) Unbalance power sharing; (f) Distortion power sharing.

After $t = 0.3s$, the master inverters are no longer supplying the balanced reactive current component except for reactive power losses over their line impedances, while the groups A and B slave inverters start supplying the balanced reactive current component of their respective local loads, with each slave providing one half as set by their respective supervisory controls.

At $t = 0.9s$, another set of load configuration in group A is switched. This means that groups A slave inverters now supplies twice reactive power compared to slave inverters in group B considering $loadA$ is now twice $loadB$. Again, there is no reactive power transfer between groups A and B, and (Q_{lineAB}) is negligible showing the inter groups line impedance reactive power losses. Due to the implementation of resistive line impedance compensation in droop control, P and Q are decoupled and changing the ratio of active power droop slope between master inverters in Fig. 8(c), has no impact on Q , as can be seen in Fig. 8(d).

Fig. 8(e) and Fig. 8(f) show the sharing of unbalance and distortion power components of the loads (N_{loadA}) and (N_{loadB}) and (D_{loadA}) and (D_{loadB}) among group A and B inverters, respectively. Until $t = 0.3s$, the master inverters supply the load unbalance and distortion power components equally without unbalance and distortion power transfer between groups A and B as the load for both groups A and B is identical, and therefore, (N_{lineAB}) and (D_{lineAB}) are zero.

After $t = 0.3s$, to improve power quality at the load buses, supervisory control in each group sets slave inverters 2 and 3 to inject the unbalance and distortion power components of the local load, respectively, as illustrated in Figs. 8(e) and 8(f). It means slave inverter 2 provides void current and slave inverter

3 supplies unbalanced current in their corresponding groups.

At $t = 0.9s$, another set of load configuration is switched on in group A meaning that groups A slave inverters now supplies twice unbalanced and distortion power components compared to slave inverters in group B. It can be seen that there is no distortion and unbalance power transfer between groups A and B, as (N_{lineAB}) and (D_{lineAB}) are zero.

It is noted from Fig. 8(c) to Fig. 8(f) that the power components supplied by slave inverter 2 in group A exhibit overshoots at $t = 0.9s$. This is because according to the CPT definitions, any disturbances in the microgrid are reflected in the void current. Since the load changes occurs in group A and the slave inverter 2 in this group is assigned to supply the void current, all the power components supplied by slave inverter 2 in group A are affected during load change at $t = 0.9s$.

It is also noted that in Fig. 8(f) the inverters void power components exhibit overshoots due to the transitions during the change of the ratio of active droop line setting for master inverters or reference current for slave inverters since these transitions are also considered as disturbances for the CPT and are reflected in void current. However, no unpredictable behavior was found to occur.

Fig. 8 depicts that the power components are shared between converters closely with the predefined share factors and during the load switching events, the disturbances are damped immediately.

C. Dynamic response of the autonomous microgrid under loads switching events

The dynamic performance of the islanded microgrid in response to sudden changes in the load is depicted in Fig. 9.

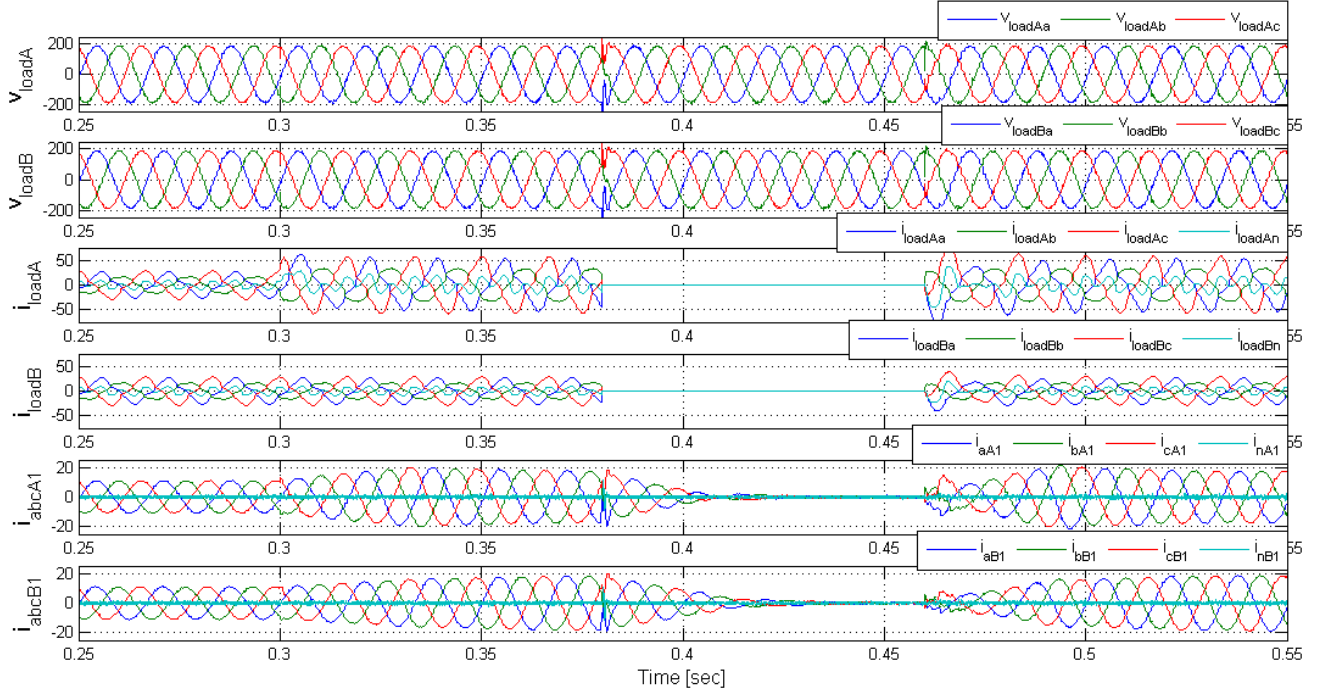


Fig. 9. Dynamic response of the autonomous microgrid to load increment in group A by twice at $t=0.3s$, when the entire load is switched off and switched on at $t=0.38s$ and $t=0.46s$, respectively with predefined sharing factors for each inverter.

This figure presents the groups A and B load buses voltages and currents and the current waveforms of groups A and B master inverters, respectively. The ratio of active droop line setting provided by the supervisory control for groups A and B master inverters are $(k_{pA1} = k_{pB1})$. To improve the load voltage quality, the provision of non-active components are carried out by the slave inverters and the master inverters only need to supply the balanced active power component which are not supplied by the slaves. This ensures a reduction in voltage THD to 2%.

In Fig. 9, the reference current provided by the group A supervisory control for the respective slave inverters are $(\underline{i}_{refA2} = \frac{1}{6}\underline{i}_a^b + \frac{1}{2}\underline{i}_r^b + \underline{i}_v)$ and $(\underline{i}_{refA3} = \frac{1}{6}\underline{i}_a^b + \frac{1}{2}\underline{i}_r^b + \underline{i}_u)$ of loadA. The reference current provided by the group B supervisory control for respective slave inverters are $(\underline{i}_{refB2} = \frac{1}{3}\underline{i}_a^b + \frac{1}{2}\underline{i}_r^b + \underline{i}_v)$ and $(\underline{i}_{refB3} = \frac{1}{3}\underline{i}_a^b + \frac{1}{2}\underline{i}_r^b + \underline{i}_u)$ of loadB. Originally in Fig. 9, the system is under identical load configurations for both groups A and B. At $t=0.3s$, another set of load configuration is switched on in group A resulting in load current increment by 100 percent in this group. It can be seen that groups A and B master inverters share the same amount of active power components as $(k_{pA1} = k_{pB1})$. At $t=0.38s$ the groups A and B load configuration is switched off; thereafter, the system operation is under the no-load condition. At $t=0.46s$ the load again is brought into operation.

Fig. 9 indicates that, despite the load switching events, the load voltage and frequency are well regulated, and the disturbances are damped immediately. Hence, the closed-loop system is robust to the changes in the loads configuration and dynamic properties.

D. Impact of communication delay on load buses voltage

While slave units have access to high-bandwidth communication links there can be some time delay or phase shift between the output current of these units and the load currents, due to communication delay [10]. However, the parallel operation in communication-based schemes is not affected if this time delay is very small [9], [10]. The previously presented simulation results have been obtained assuming 0.1ms delay of high-bandwidth communication between the slave and the supervisory control [9]. The latency is simulated by using time delay blocks. In Fig. 10, the effect of this delay on the load buses voltages is investigated by implementing a larger delay due to the communication technology used, namely 10ms at $t=0.3s$.

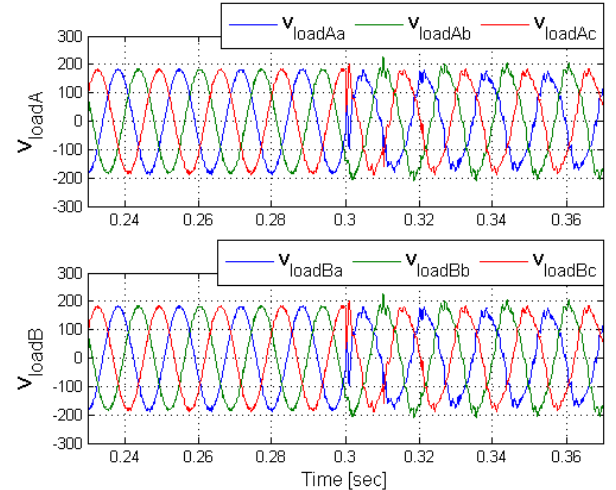


Fig. 10. Effect of communication delay on Groups A and B load buses voltage waveforms after ($t=0.3s$).

It is observed that a large delay can deteriorate the operation of slave units due to phase shift between the output current of each slave unit and load current in each group and leads to distortion of the load buses voltages.

V. CONCLUSIONS

The close proximity makes it practical for control signals to be communicated between inverters with the potential to provide rapid load sharing for mitigation of unwanted current components of nonlinear and/or unbalanced loads. However, due to impracticality of communication between inverters at remote nodes, sharing between these groups is accomplished through voltage and frequency droop methods. This paper proposes a multi-master-slave-based control of DGs in a three-phase four-wire islanded microgrid in which inverters located in close proximity operate as a group in master-slave mode to inject the available energy and provide rapid load sharing for mitigation of non-active current components of local loads with the secondary effect of the enhanced voltage quality at master inverters terminal and load buses while sharing the remaining load power with distant groups based on the ratings and availability of primary energy sources using conventional frequency droop.

The main functionalities are based on CPT decomposition, which adds significant flexibility to the system, especially when the instantaneous capability of the inverter is limited. Beyond its flexibility and selectivity, CPT does not require any kind of reference-frame transformation. Due to complex values of the line impedance, which leads to coupling of active and reactive power droop controls, compensation of resistive line impedance is implemented to make the line impedance appear to the converter as purely inductive impedance which enables decoupled control of those power terms.

Simulation results verify the effectiveness of the proposed cooperative control with satisfactory voltage quality improvement. In case of the load changes, as proved, the load voltage and frequency are well regulated, and the disturbances are damped in a reasonable response time. The authors expect this solution can be retrofitted to many existing distribution grids. Note that if the slaves just compensated part of the non-active current, the master units will share the remaining non-active currents accordingly.

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